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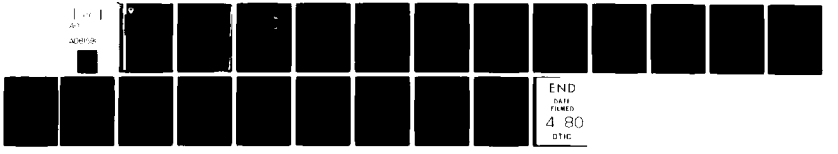

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AN/TPQ-37 TRANSMITTER TEST BED

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FEBRUARY 1980

Second Interim Report for Period February 1979 Through July 1979

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The AN/TPQ-37 Transmitter Test Bed will provide a vehicle for evaluating techniques for improving the reliability and maintainability of the AN/TPQ-37 Transmitter. Work includes design and fabrication of a major portion of the microprocessor based fault isolation subsystem.

Support has been provided to ERADCOM in monitoring procurement of Advanced Design Traveling Wave Tubes. During a later phase of the program these TWT's will be evaluated in the AN/TPQ-37 Transmitter.

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SUMMARY

The AN/TPQ-37 Transmitter Test Bed will provide a vehicle for evaluating techniques for improving the reliability and maintainability of the AN/TPQ-37 Transmitter. Work includes design and fabrication of a major portion of the microprocessor based fault isolation subsystem.

Support has been provided to ERADCOM in monitoring procurement of Advanced Design Traveling Wave Tubes. During a later phase of the program these TWT's will be evaluated in the AN/TPQ-37 Transmitter.

Progress during this reporting period on the AN/TPQ-37 Test Bed Program includes:

- Design of fault isolation firmware.
- Coding and testing of fault isolation firmware needed for the interim transmitter tests scheduled for August.
- Fabrication of mounting and installation hardware for interfacing the fault isolation circuits to the transmitter.
- Design and fabrication of transformer case needed for the new solid state modulator.
- Design of new inverter commutating choke and placing of purchase orders for material required for fabrication.

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Section 1

INTRODUCTION

1.1 PROGRAM OBJECTIVES

The AN/TPQ-37 Transmitter Test Bed will provide a vehicle for evaluating techniques for improving the reliability and maintainability of the AN/TPQ-37 transmitter.

The specific objectives of this program are:

1. To evaluate Advanced Design Traveling Tubes resulting from USAERADCOM solicitation DAAB07-78Q-2082.
2. To design, develop, and evaluate in a AN/TPQ-37 transmitter a microprocessor based fault isolation subsystem that will report malfunctions in a maintenance oriented manner.
3. To design, develop, and evaluate a closed loop automatic cathode current control loop.
4. To design, develop, and evaluate an automatic RF drive level control loop.
5. To evaluate in an AN/TPQ-37 transmitter the solid state floating deck grid modulator developed under contract DAAB07-77-C-2647.
6. To design, develop, and evaluate an improved inverter commutating choke.

1.2 PROGRAM ORGANIZATION

The objectives of this program will be accomplished in three major phases:

The first phase will include the independent development and testing of the new components and circuits, which include:

- Support procurement of an advanced design TWT.
- Design a new, cased transformer for use with the solid state grid modulator.
- Fault isolation circuits and control loop circuits.
- Improved commutating choke design.

The second phase will consist of two separate transmitter tests. The first of these tests is scheduled for August through October 1979 and the final test is scheduled for May 1980 through January 1981. The first of these test periods will evaluate those portions of the microprocessor based fault isolation system associated with the inverter power supply, and floating deck grid modulator and one Varian TWT. Evaluation of the remainder of the circuitry and TWT's will be deferred to the second test period.

The last phase will include development of recommendations accumulated during the test phase and presentation of the recommendations in the final report.

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The last phase will include development of recommendations accumulated during the test phase and presentation of the recommendations in the final report.

Section 2

PROGRESS

2.1 ADVANCED DESIGN TRAVELING WAVE TUBE

Program reviews have been conducted jointly with ERADCOM at both Varian Associates and Hughes Electron Dynamics Division to monitor their approaches to achieve TWT improvements. Both companies have completed assembly and evaluation of electron gun test vehicles. Varian's evaluation demonstrated satisfactory operation, but EDD's triodes did not demonstrate the anticipated reduction in cathode operating temperature. Varian has also completed fabrication of the first complete TWT and is completing their evaluation of the TWT.

2.2 FAULT ISOLATION

During the first reporting period the circuits needed for detailed fault isolation were designed and fabricated, and initial testing was begun. During this, the second, reporting period the overall fault isolation firmware was designed. The firmware needed to support the interim tests has also been coded and tested, and is ready for use during the first transmitter test period.

2.2.1 Fault Isolation Hardware. The fault isolation hardware (block diagram is shown in Figure 1) consists of a microprocessor based fault controller card, a video display and three transmitter interfacing circuits. These circuits, as described in the first interim report, enable the fault isolation logic to track the transmitter through its turn on and operational sequences and detect and report fault conditions.

2.2.2 Fault Isolation Firmware. The fault isolation firmware is made up of four functional groups as shown in Figure 2:

- Initialization. This portion provides startup conditions for both hardware and firmware.
- Data Collection. This group controls the interface to the transmitter sensors that provide pertinent operating data.

- Error and Status Reporting. Serial data to the video display is provided by this group. This data is used for fault reporting and for manual verification of monitor circuits.

- Fault Detection. This portion tracks the transmitter's turn on and operating sequences, and detects deviations from normal.

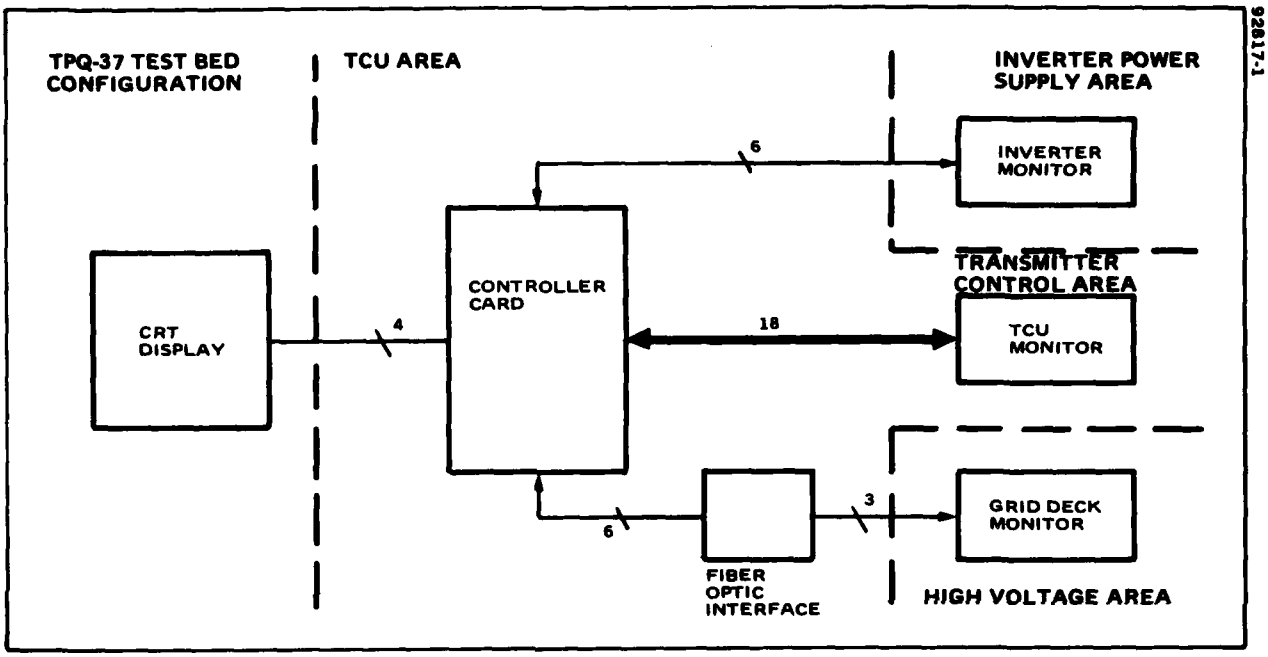

Figure 1. Fault Isolation Subsystem Block Diagram

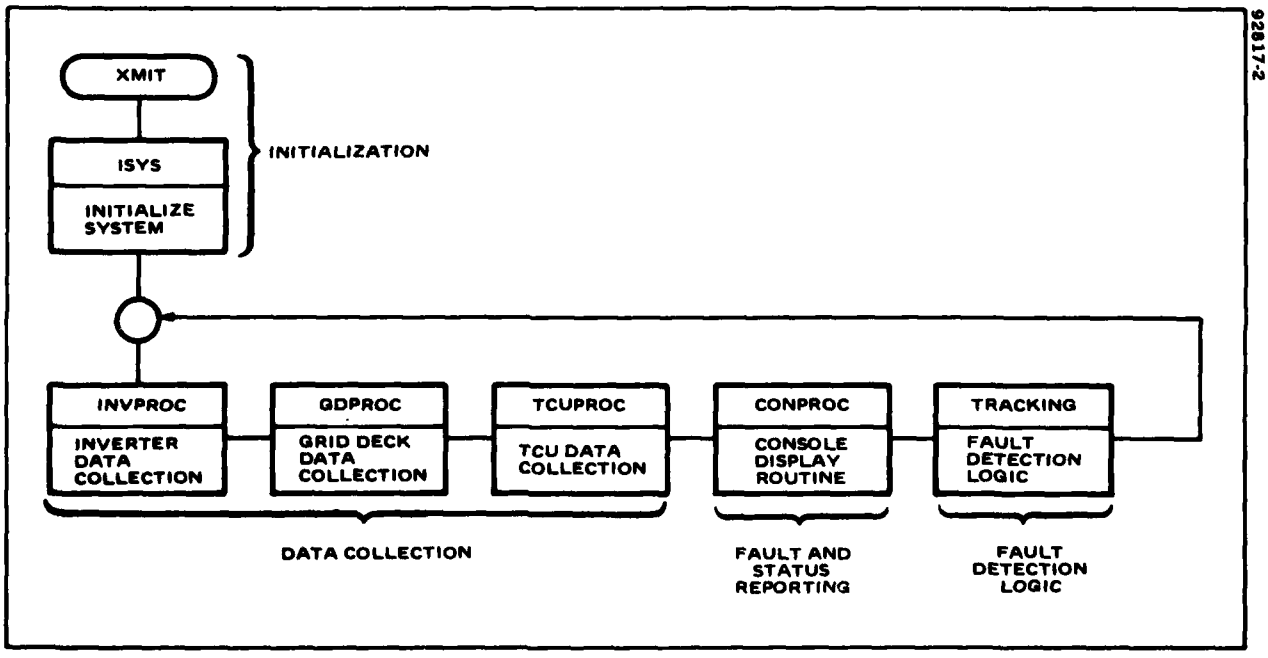

Figure 2. Main Fault Isolation Control Loop

Section 3

FAULT ISOLATION TECHNIQUES

3.1 INTRODUCTION

The techniques to be used for transmitter fault isolation are similar to those used by maintenance personnel. That is, a trained operator expects certain reactions to external stimuli in order to verify the operation of the transmitter. Any deviation from the expected reaction provides valuable information to the operator as to the possible cause of the problem. It is this technique which is expanded upon in the fault isolation firmware logic.

The fault isolation subsystem will take advantage of, and in fact expand on the functional isolation provided by transmitter sequencing. That is, for any step in a sequence to be initiated, prior steps must have been successfully completed. This implies that the required circuits performed their function. Alternately if a step in the sequence failed to produce the expected results, only those circuits responsible for the functional step need be considered. It can be shown that reducing the functional complexity of each step in the sequence reduces the amount of circuitry to be considered by the fault isolation firmware.

The firmware in the controller card will use the status information provided by the transmitter monitor cards. The microprocessor will determine the current step or state and test for the expected result.

The functional isolation of the circuitry permits us to develop equations relating a fault to its possible causes. When a fault is detected these equations are used to further isolate the fault to a LRU.

3.2 FAULT ISOLATION FIRMWARE

The fault isolation firmware provides control of both fault detection and reporting. It consists of about 50 sub-programs and 6 data tables, and uses about 16,000 bytes of microprocessor memory. The major goal of the design is to isolate the faulted hardware down to the line replaceable unit (LRU). The firmware also provides control of the TWT cathode current and RF drive, and thus maintain optimum operating conditions.

3.2.1 Initialization. At turn on, all hardware and firmware variables are initialized. In addition, a sequence of self-test routines is performed to verify correct operation of the controller hardware.

3.2.2 Console Processing. The Console Processing routines provide continuously updated status information to the console display. Both raw status information collected from the monitor circuits and the current fault isolation status are displayed. The raw data is then used to manually verify the results of the fault isolation logic.

3.2.3 Inverter Processing. The inverter processing routines control the serial interface between the controller card and the inverter monitor. This bi-directional interface carries data both to and from the inverter. The data received from the inverter includes analog and digital status information. This data is used by the console processing for display, as well as by the fault isolation logic for fault detection. The interface to the inverter is currently used only for self test, although it could eventually be used for inverter control.

3.2.4 Grid Deck Processing. The grid deck processing program controls the serial interface between the controller card and the grid deck monitor. As in the inverter, serial interface data is transmitted bi-directionally. Data from the grid deck is used for both display at the console and for fault detection. Data to the grid deck is used for self test as well as to provide control of the TWT cathode current.

3.2.4.1 First Fault Logic. In addition to raw status data, first fault information is also collected from the grid deck. The first fault logic is a latching circuit which is enabled only after all fault conditions have been cleared (i.e., when the transmitter is correctly operating). Once enabled, this circuit latches status information just as the first fault is detected, thus preserving information which would be otherwise lost due to the subsequent fault activated shutdown.

3.2.5 TCU (Transmitter Control Unit) Processing. The TCU processing routines control the parallel interface between the controller card and the TCU monitor card. This bi-directional parallel interface is used to transmit both digital and analog data to and from the TCU monitor.

The status information collected by the TCU Processing is used to update console status displays as well as provide input to the fault detection logic. This information also provides data for use in the cathode current and RF drive control loops.

3.2.6 Fault Detection Logic. The fault detection logic uses information gathered by the data collection routines to track the transmitter through its normal sequences. By testing for key transitions of its status information, the fault detection logic can detect fault conditions and report their probable causes.

Section 4

SOLID STATE GRID MODULATOR

An attempt to redesign the pulse transformer to achieve any significant decrease in rise time was not successful. Various coil and core configurations were tried which would decrease the transformer parameters: such as leakage inductance and distributed capacity. Although those parameters could be reduced, the high voltage isolation requirements, the high value of load resistance and the high value of load capacitance preclude any decrease in rise time beyond approximately two percent. As a result of this study, it was decided to proceed with the mechanical design of a housing for the existing transformer. Fabrication of this housing is presently in work.

Section 5

COMMUTATING CHOKE DESIGN

The current AN/TPQ-37 transmitter beam power supply design incorporates an SCR inverter network that is self commutating due to the resonant effects of a commutating choke and commutating capacitor. The present commutating choke is an air core design with a nominal inductance of 16 microhenries. Because of the air core design, substantial magnetic fields are produced and coupled to surrounding support structures and circuitry, causing unwanted induction heating and noise problems. Also the air core choke requires water cooling.

A new iron core commutating choke has been designed for the test bed program and is being fabricated for evaluation in the test bed transmitter. The new iron core choke was designed to significantly reduce the induced heat and circuit noise generated by the air core design. Proper choice of conductor dimensions, coil configuration, and air gaps are used to reduce eddy current losses and eliminate the need for water cooling.

Section 6

AUTOMATIC CONTROL LOOPS

6.1 AUTOMATIC CATHODE CURRENT CONTROL

The automatic cathode current control loop (CCCL) as described in the first interim report requires the use of the TCU monitor portion of the fault isolation system. This portion of the system is scheduled to be tested in May of 1980; hence the CCCL will also be tested at that time.

6.2 AUTOMATIC RF DRIVE LEVEL CONTROL LOOP

It was originally planned to continuously monitor and control the TWT RF drive level in order to operate the tube just in saturation at all times. This would maintain the correct output power from the TWT, as well as reduce the possibility of overdrive. While these would be ideal conditions for the TWT, the RF phase changes resulting from the drive level changes could interfere with the effectiveness of the radar signal processing. For example, the technique of dithering the drive slightly during operation to find the optimum point at each new operating frequency is entirely acceptable in a system where the frequency is not changed for a very large number of transmitter pulses. However, in a system such as the AN/TPQ-37, where the frequency is changed at the start of each dwell, the number of pulses degraded in stability would represent a significant percentage of those processed, and would result in unacceptably degraded moving target performance.

One approach that has been suggested involves special routines incorporated in the system software. In this approach, at each cold start, the system would provide a short burst of calibration pulses to the transmitter at each possible RF frequency. The transmitter microprocessor (using the dithering technique) would use these pulses to determine the optimum drive level for each frequency, and store this data in a table in the microprocessor memory. Then, during actual system operation, the system computer would provide the transmitter with the next operating frequency during the inter-dwell period. From this information, the microprocessor would set the RF drive attenuator to the appropriate value for the upcoming dwell. Since the data table is generated freshly each time the system is turned on, the effects of long term aging are accounted for. And, of course, the possibility of manual mis-adjustment of the drive level is eliminated.

This approach has been discussed with the AN/TPQ-37 systems engineers. The computer already has a digital word available describing the next intended transmit frequency. It would only require addition of a wire to the transmitter, and coding of the calibration routine to implement this scheme. It is planned to further evaluate this approach and to implement the circuitry and software so loop operation can be evaluated during the second test period.

Section 7

TRANSMITTER TEST BED EVALUATIONS

7.1 INTERIM TESTS

The transmitter test bed program testing will initially make use of AN/TPQ-37 transmitter number 4 from August through October of 1979. During the interim tests, much of the new hardware and firmware developed under this contract will be tested and evaluated. These tests will provide sufficient lead times to correct design anomalies prior to final tests commencing in May of 1980.

The first interim tests will include the installation and testing of most of the fault isolation hardware and firmware, one new Varian TWT, and the solid state grid modulator.

7.2 FINAL TESTS

Items to be tested starting in May of 1980 are the fault isolation TCU monitor, control loops and the remainder of the fault isolation firmware and the remaining improved TWTs.

Section 8

CONCLUSION

During the second reporting period the fault isolation hardware and much of the firmware has been completed and bench tested. The components needed for evaluation during the interim tests commencing in August of 1979 are ready for installation in the transmitter. Components needed for installation of the new solid state grid modulator have also been fabricated and are awaiting assembly and tests. Finally, one of the new Varian TWT's is expected to be available for testing during the interim test period.

Section 9

SUBSEQUENT PROGRAM DIRECTION

Evaluation of much of the new hardware and firmware will start in August of 1979 in AN/TPQ-37 transmitter 4. These tests will provide the basis for concluding the design, leading to final tests beginning in May of 1980.

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